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Design of 1 V Operating Fully Differential OTA Using NMOS Inverters in 0.18 μm CMOS Technology*

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SUMMARY This paper presents a 1 V operating fully differential OTA using NMOS inverters in place of the traditional differential pair. To obtain high gain, a two-stage configuration is used in which the first stage has feedforward paths to cancel the common-mode signal, and the second stage has common-mode feedback paths to stabilize the output common-mode voltage. The proposed OTA was fabricated by an 0.18 μm CMOS technology. Measured gain is 40 dB and GBW is 10 MHz, in addition to differential output voltage swing of 1.8 $V_{p\text{-}p}$. It is confirmed that the proposed OTA can operate from 1 V power supply and has very large output swing capability even in a 1 V operation. The proposed OTA configuration contributes to a solution to the low power supply voltage issue in scaled CMOS analog circuits.

key words: *low power supply voltage, large output swing, fully differential OTA, NMOS inverters*

1. Introduction

In recent years, mixed analog-digital circuits have become main-stream technology for enhanced performance, smaller chip area, and cost reduction. In digital circuits, down scaling of technologies have advanced circuit performances. With down scaling of technologies, the power supply voltage must be lowered. This has been predicted by the International Technology Roadmap for Semiconductors (ITRS) as shown in Fig. 1 [1].

In analog circuits, the operation from low power supply voltages becomes necessary to realize mixed analog-digital circuits. An operational transconductance amplifier (OTA) is a basic block of analog circuits and is used in filters, A/D converters, D/A converters etc. However, it is difficult to operate from low power supply voltages for a traditional OTA using the differential pair. Several ideas have been proposed to use CMOS inverters in place of the differential pair in order to lower its operating voltage [2], [3]. However, CMOS inverters require two threshold voltages or more, at least, for the power supply voltage to operate properly. On the other hand, it is possible for NMOS inverters to operate from lower power supply voltages than CMOS inverters. Actually, a 0.9 V operating fully differential OTA using NMOS inverters has been reported [4]. However, the OTA cannot control its common-mode output voltage by itself, because it has only feedforward paths to cancel input common-mode signals. On the other hand, the cascade connection of a feedforward OTA and a feedback OTA configuration (F/F+F/B OTA) [3] can control and maintain its output common-mode voltage at a desired level, e.g, at the half of the power supply voltage, by common-mode feedback.

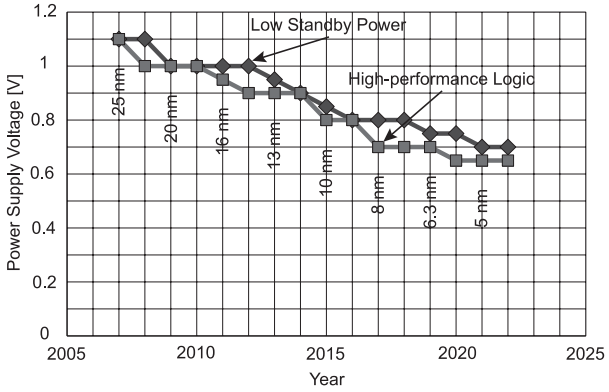

Fig. 1 Power supply voltage trend (ITRS roadmap).

In the near future, the operation of an OTA from 1 V power supply will be indispensable according to Fig. 1. Therefore, we designed and fabricated a 1 V operating fully differential OTA using NMOS inverters in place of CMOS inverters in the F/F+F/B OTA. Simulated and measured results are presented.

2. Issues in Low Power Supply Voltage Operation

A traditional OTA uses the differential pair. The differential pair is shown in Fig. 2. This configuration has three stacked MOSFETs between V_{DD} and GND. The drain-source voltage $V_{DS(sat)}$ is necessary so that a MOSFET operate in the saturation region. A large output swing is not possible in 1 V power supply, because $V_{DS(sat)}$ typically becomes about several hundreds of millivolts. It is difficult for the differential pair to operate from power supply voltages as low as 1 V. To overcome this situation, we adopt circuits with less number of stacked MOSFETs.

There has been some ideas using CMOS inverters in place of the differential pair to lower its operating voltage [2], [3]. The CMOS inverter is shown in Fig. 3. This configuration has only two stacked MOSFETs between V_{DD} and GND, so that the output swing of the CMOS inverter is larger than that of the differential pair. However, CMOS inverters still require at least two threshold voltage ($2V_{th}$) to operate in the input side so that the operation below 1 V may

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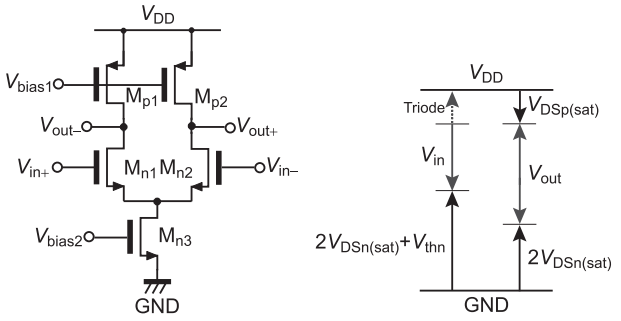

Fig. 2 Differential pair.

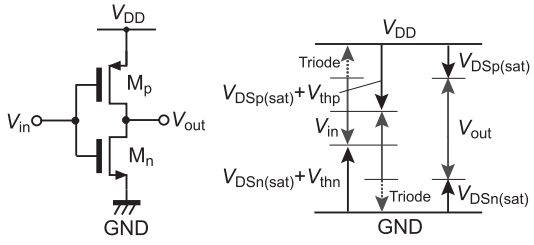

Fig. 3 CMOS inverter (C-INV).

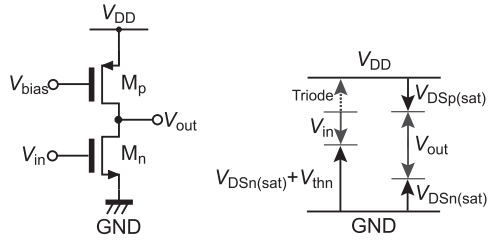

Fig. 4 NMOS inverter (N-INV).

not be easy.

It is possible to lower V_{th} by using additional processing steps; however, it is not practical from the view point of increased production cost and leakage currents in digital circuits. Thus, we decided to adopt simple NMOS inverters, instead of CMOS inverters, without changing V_{th}.

The NMOS inverter is shown in Fig. 4. The use of a PMOSFET as a load current source makes it possible to determine the NMOS inverter's bias current independent of V_{th} of the NMOSFET. Therefore, it is possible for NMOS inverters to operate from lower power supply voltages than CMOS inverters. However, the input range of the NMOS inverter reduces in the lower portion as shown in Fig. 4.

The right sides of Figs. 2∼4 show the input and output range, where broken lines with "Triode" indicate that the N/PMOS enters the triode region.

3. Fully Differential OTA

3.1 Basic Idea

A circuit configuration of the F/F+F/B OTA is shown in Fig. 5 [3]. First, this OTA forms a fully differential OTA,

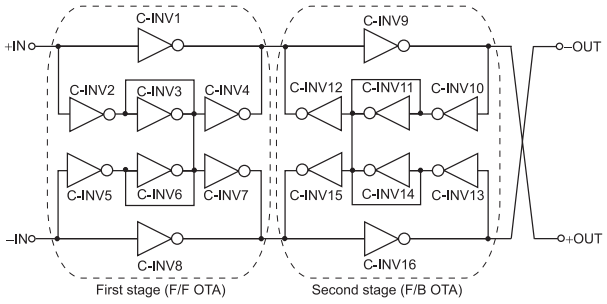

Fig. 5 Circuit configuration of the F/F+F/B OTA.

in order to obtain a large output signal swing and reduce susceptibility to common-mode noises. The output swing of a fully differential OTA is a double of that of a single-ended OTA. Next, this OTA composes a two-stage OTA, in order to obtain high gain. We could obtain only about 20 to 30 dB of gain, if we used a single-stage configuration. This is because of low output impedance of an 0.18 μm CMOS technology for the minimum gate length.

To suppress the common-mode gain, this OTA has feedforward paths and feedback paths, in order to operate as a fully differential OTA. The first stage has feedforward paths to cancel common-mode input signals, while the second stage has common-mode feedback paths to stabilize the output common-mode voltage. The input common-mode signal is detected by averaging two inverted input signals, and only the inverted common-mode signal is fedforward via two replica inverters (C-INV4, C-INV7) to the inverters in main signal paths (C-INV1, C-INV8). Likewise, the output common-mode signal is also detected by averaging two inverted output signals, and only the inverted common-mode signal is fedback via two replica inverters (C-INV12, C-INV15) to the inverters in main signal paths (C-INV9, C-INV16). Hence, the differential-mode signals are not fedforward nor fedback because of the averaging action. This is shown in Fig. 6(a).

Our main idea is to replace the CMOS inverters with NMOS inverters; however, simple replacements cause a problem. In the averaging stages, the differential-mode signals may not perfectly cancel out, due to its class-A operation of the NMOS inverters. This is shown in Fig. 6(b). This causes the differential-mode output voltages to clip in its upper half portion, because some of the differential-mode signals are fedforward and fedback, and lowers the differential-mode gain. This never occur when using CMOS inverters.

To solve this problem, we decline to use the NMOS inverters to average in the first stage (F/F OTA) and the second stage (F/B OTA).

3.2 First Stage Design

We decline to use the averaging action at the F/F OTA by disconnecting the outputs of N-INV3 and N-INV6, and the feedforward paths are cross connected to N-INV8(N-INV1) from N-INV4(N-INV7) as shown in Fig. 7(b).

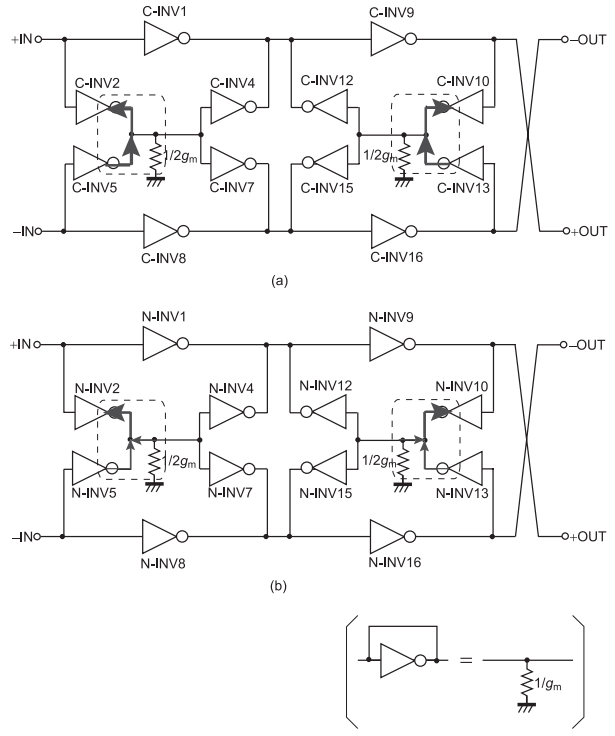

Fig. 6 Flow of the differential-mode signals of the F/F+F/B OTA using CMOS inverters (a), and using NMOS inverters (b).

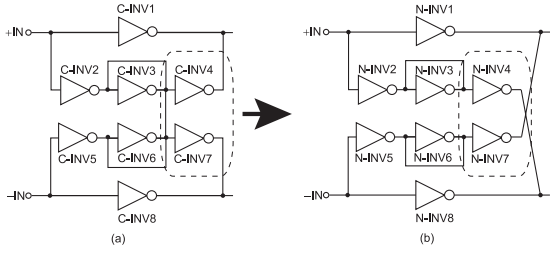

Fig. 7 First stage of before (F/F OTA) (a), and after (cross F/F OTA) (b).

This permits signals to feedforward both common-mode and differential-mode; however, only the common-mode signals are canceled and the differential-mode signals add due to the cross connection around the feedforward paths. The differential-mode gain of the cross F/F OTA is a double of that of the conventional F/F OTA.

3.3 Second Stage Design

We adopted the F/B OTA in the second stage. A resistive averaging circuit is used in front of the feedback circuit which consists of NMOS inverters (N-INV10∼13) as shown in Fig. 8(b). This eliminates the differential-mode signal inputs to the feedback circuit, and only the common-mode feedback remains. The resistance of the averaging circuit must be much larger than the output resistance of the main forward path inverter N-INV9(N-INV14) in order to keep the gain high.

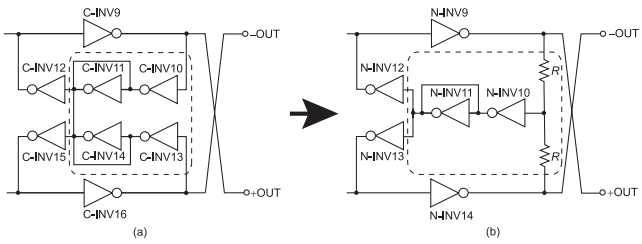

Fig. 8 Second stage of before (F/B OTA) (a), and after (F/B OTA with resistive common-mode detector) (b).

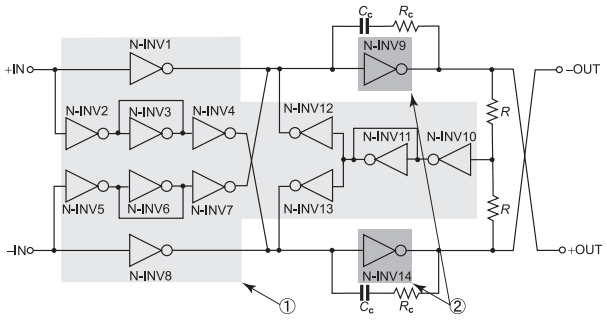

Fig. 9 Circuit configuration of the proposed OTA.

Table 1 Transistors and other elements of the proposed OTA.

Item	Value
$W_p/W_n/L_{p,n}$ (part ①)	6 μm/1.5 μm/0.18 μm
$W_p/W_n/L_{p,n}$ (part ②)	60 μm/15 μm/0.18 μm
R	220 kΩ
C_c	2 pF
R_c	1 kΩ

3.4 OTA Design

The proposed OTA is a cascade connection of the cross F/F OTA and the F/B OTA with resistive common-mode detector as shown in Fig. 9. We assume an 0.18 μm CMOS technology in this design. The gate lengths L of the NMOS inverters are 0.18 μm (minimum dimension) considering speed and power dissipation. The gate widths W of the NMOSFETs are designed to be 1.5 μm, and those of PMOSFETs are designed to be 6 μm. The first stage inverters have all the same aspect ratio to keep the common-mode cancellation high (Table 1).

In the second stage, main forward path inverters (N-INV9, N-INV14) have ten times the larger gate widths than the first stage inverters, because they must provide larger output currents. Other inverters are of the same dimension as that of the first stage. Each unit inverter consumes about 5 μA, and the output stage inverter consumes about 50 μA from 1.0 V power supply. Total current consumption is about 170 μA. The resistance R of the averaging circuit is 220 kΩ, because the estimated output resistance of N-INV9(N-INV-14) is 22 kΩ (Table 1).

Because the proposed circuit is a two-stage amplifier,

we introduced a conventional Miller compensation at the second stage as shown in Fig. 9. The compensation capacitor C_c is 2 pF, and resistor R_c of 1 kΩ is put in series, in order to obtain phase margin of about 60 degrees. Simulated gain is 44 dB, and GBW is 13 MHz for no-load condition.

4. Simulated and Measured Results

The proposed OTA was designed and fabricated by using TSMC 0.18 μm 1P6M mixed signal CMOS technology. A micrograph of the fabricated OTA is shown in Fig. 10. The size of the fabricated OTA is 315.5 μm $\times$ 193.8 μm. The large area of the right side is occupied by resistors of the averaging circuits (2 $\times$ 220 kΩ).

The proposed OTA is measured by using an impedance analyzer via a high impedance FET probe. In the differential-mode measurement, a signal was input into only one port as shown in Fig. 11 (a), because this OTA has a large common-mode rejection ratio. In the common-mode measurement, input ports and output ports were tied respectively to measure their common-mode components as shown in Fig. 11 (b).

Figure 12 shows the simulated and measured frequency responses of the proposed OTA. For the differential-mode, the simulated gain is 42 dB and the measured gain is 39 dB for a 100 kΩ load with a 13 pF capacitor in parallel. For the common-mode, the simulated gain is -33 dB and the measured gain is -35 dB for the same condition. These results indicate that the measured amplitude responses are well matched with the designed responses.

The common-mode phase response could not be measured. The measurements for the common-mode signal is difficult because the common-mode signal is very small due to a very large common-mode rejection ratio of the proposed OTA. However, because the measured common-mode gain is less than unity for all frequency range, a stability problem will not occur. Anyway, the measured results indicate its usefulness of the proposed OTA operating at low power supply voltage situation.

Figure 13(a) shows measured output clipping levels to show the maximum output voltage swing capability of the two outputs. Each output voltage swings 880 $mV_{p\text{-}p}$ at 1 V power supply, as expected from the simulation result. Figure 13(b) shows the maximum differential output voltage swing, which is 1.8 $V_{p\text{-}p}$ at 1 V power supply. It has been confirmed that the proposed OTA has a very large output swing capability even in a low power supply voltage.

The simulated and measured performances of the proposed OTA are summarized in Table 2. Unfortunately, its current consumption was not measured, because the power supply line is common to other circuits on the same chip.

5. Discussion

First, we discuss the differential-mode gain. The gain of the proposed OTA is about 40 dB in the gate lengths of NMOS inverters are 0.18 μm (minimum dimension). This gain value is not so large. The gate lengths should be made large while maintaining the aspect ratio to obtain high gain. Sim-

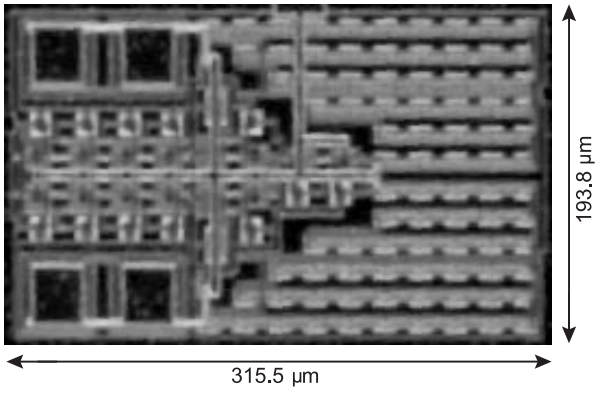

Fig. 10 Chip micrograph of the proposed OTA.

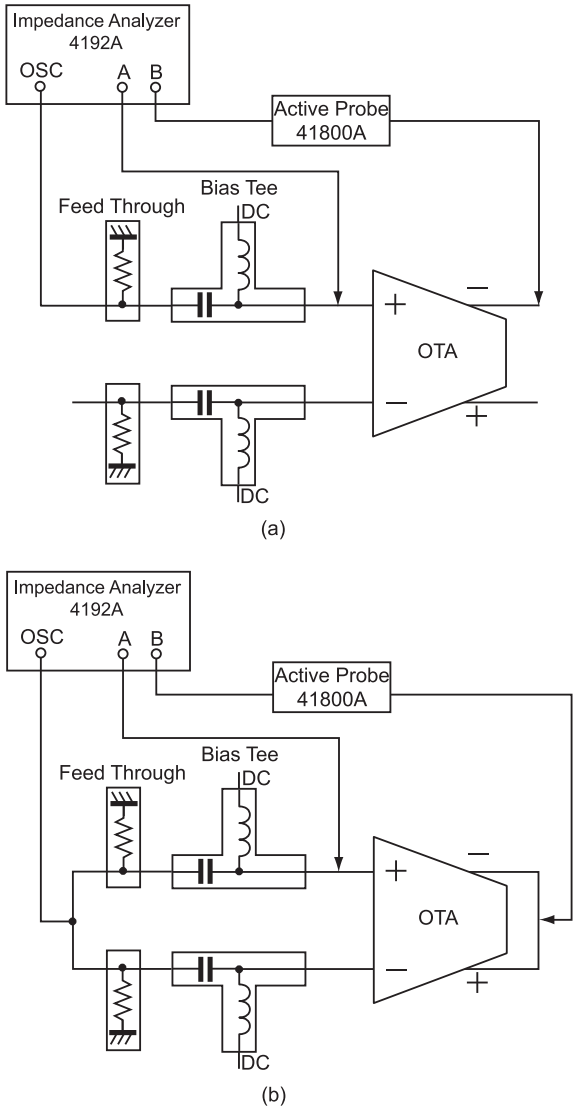

Fig. 11 Measurement setup for OTA of the differential-mode (a), and of the common-mode (b).

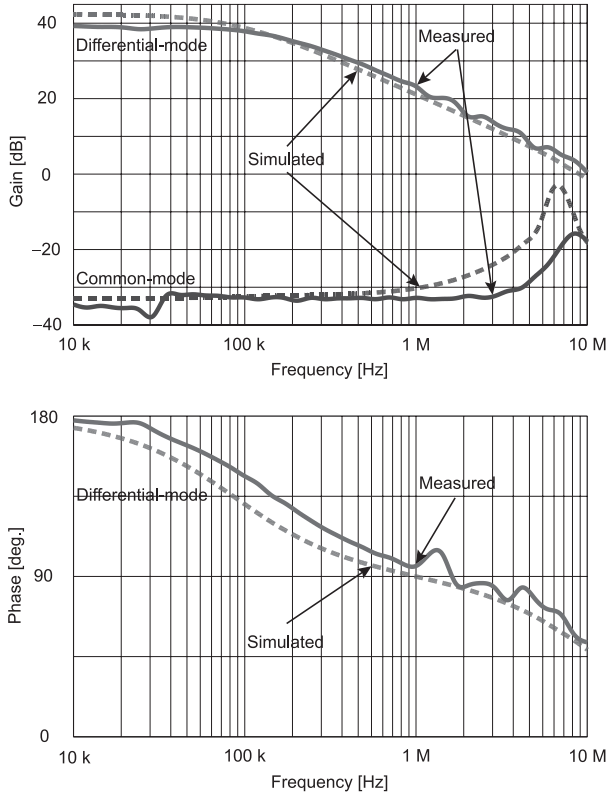

Fig. 12 Bode plot of the proposed OTA.

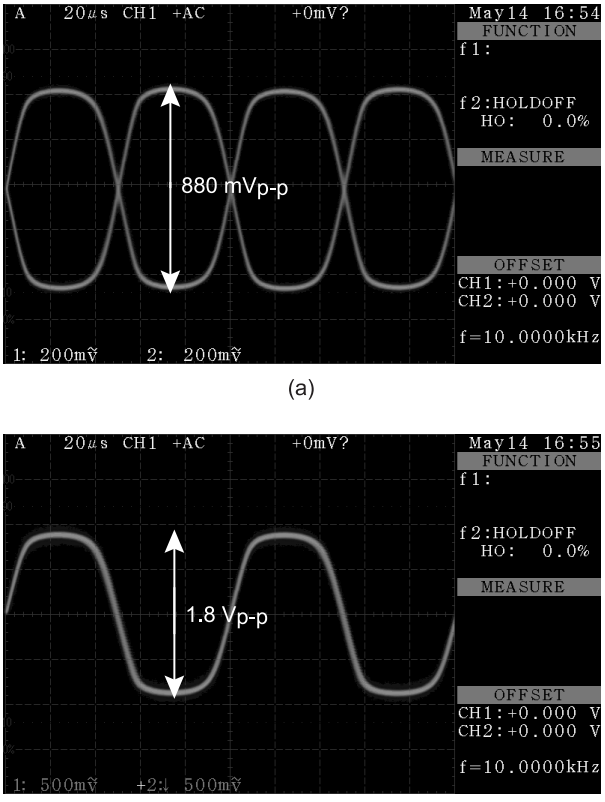

Fig. 13 Measured output swing of the proposed OTA. Two single-end output voltages (a), and differential output voltage (b).

Table 2 Performance summary of the proposed OTA.

Item	Simulated	Measured
Power supply voltage	1.0 V	1.0 V
Current consumption	170 μA	—
Open-loop dc gain	42 dB	39 dB
Cutoff frequency	88 kHz	120 kHz
GBW	9 MHz	10 MHz
Phase margin	52 deg.	53 deg.
Output voltage swing	28–974 mV	50–930 mV
CMRR @10 kHz	75 dB	74 dB
PSRR @10 kHz	46 dB	—

*R_L=100 kΩ, C_L=13 pF

ulation indicates that we could have obtained about 70 dB of gain, if the gate lengths were designed to be 0.5 μm.

Next, we discuss the peak of the common-mode gain response in Fig. 12. In this measurement, a stability problem will not occur, because the measured common-mode gain is less than unity for all frequency range. However, it could lead to an instability when process and/or temperature variations are taken into account. The cause of the peak is that the compensation is not adequate for the common-mode loop. There are four inverters in the common-mode feedback loop, in which two inverters are used to obtain a gain of -1. In addition, the resistors of the averaging circuit consist a lowpass filter with parasitic capacitors at the input node of N-INV10. Those additional stages and the LPF decrease the phase margin. Compensation capacitors can be put in parallel with averaging resistors to introduce a phase-lead. Simulation results show that 3 pF of compensation capacitors are adequate for eliminating the gain peak.

We discuss the biasing condition of NMOS inverters. In this design, $V_{\rm bias}$ of all the NMOS inverters were connected to the output common-mode voltage, in order to the output common-mode voltage automatically sets to the half of the power supply voltage. However, the operating current can be controlled if $V_{\rm bias}$ is given externally. A variable $G_{\rm m}$ OTA can be realized by changing its operating current, and may be applied to variable $G_{\rm m}$-C filters.

The simulated PSRR at 10 kHz is 46 dB. This low value is attributed to the connection of $V_{\rm bias}$ with the output common-mode voltage, i.e. $V_{\rm DD}/2$. This connection makes the bias current sensitive to $V_{\rm DD}$ variation. A circuit simulation shows that if we used a traditional current-mirror circuit with the diode-connected MOS and a series resistor put in-between $V_{\rm DD}$ and ground, we could have obtained 61 dB of PSRR.

Next, we discuss the change in current consumption with temperature. The simulated total current consumption is 115 μA, 170 μA, 313 μA for 0°C, 27°C, 85°C, respectively. The current change with temperature is large, because we adopted a simple current source biasing circuit with a voltage reference at $V_{\rm DD}/2$. This may be improved by replacing the bias circuit with a temperature compensated biasing circuit or a constant $g_{\rm m}$ biasing circuit [6].

It may be informative to analyze an expected input offset voltage of the proposed OTA. The result predicts the input offset voltage to be about $\sqrt{8}$ times larger than that of the

traditional differential pair. The following is an outline of the analysis.

Because the proposed OTA is a two-stage configuration, the input offset voltage is dominated by the first stage. Then, we analyze only the first stage. Now, we assume that all the inverters have the same input offset voltage variation ΔV_{os}. Due to the symmetry of the circuit, we treat only the upper half circuit.

There are one inverter in the main signal path, and three inverters in the feedforward path. The first two of the three inverters consist a $-1\times$ amplifier, so that they have two ΔV_{os}'s in front of the last inverter, which again has one ΔV_{os}. Those offsets result in a corresponding output current, which is referred to input side by their transconductance, so that we have the input offset voltage of four independent ΔV_{os}'s. Because we have another four independent ΔV_{os}'s in the lower half circuit, we have $\sqrt{8}\Delta V_{os}$ in total as an rms value. If we assume further that the $\Delta V'_{os}$ of NMOS and PMOS are the same for simplicity, the total input offset voltage becomes $\sqrt{16}\Delta V'_{os}$, while the traditional differential pair has $\sqrt{2}\Delta V'_{os}$ of the input offset voltage. Thus, the proposed OTA has about $\sqrt{8} \approx 2.8$ times lager input offset voltage, than the traditional differential pair.

6. Conclusion

We proposed a fully differential OTA using NMOS inverters, which can operate from 1 V power supply. The proposed OTA has been designed and fabricated in an 0.18 μm CMOS technology. The measured results confirmed that the proposed OTA can successfully operate from 1 V power supply with gain of about 40 dB and GBW of about 10 MHz at current consumption of about 170 μA. It has been also confirmed that the proposed OTA has a very large output swing of 1.8 $V_{p\text{-}p}$ even in 1 V power supply. This OTA provides a solution to the low power supply voltage issue in scaled CMOS analog circuits.

The differential-mode gain of the designed OTA is lower compared with that of the reference [3]; however, we can improve its gain by using larger gate lengths. This is a future work.

The proposed OTA can operate from lower power supply voltages than the reference [3], and has better control over current consumption, in principle, because it is based on class A inverters unlike class AB CMOS inverters in the reference [3]. The proposed OTA may be applied to integrated variable filters because its transconductance can be controlled by changing its operating current.

Although the proposed OTA has both feedforward paths and feedback paths, a two-stage OTA can be realized with only feedback paths to suppress the common-mode gain and stabilize the output common-mode voltage. With such a configuration without feedforward paths, the power consumption decreases because the number of NMOS inverters decreases. This type of OTA is under study.

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