Noname manuscript No.
(will be inserted by the editor)

A Fully-Differential OTA Based on CMOS Cascode Inverters Operating From 1-Volt Power Supply

Hiroshi Tanimoto · Kazuki Yazawa · Masaru Haraguchi

Received: date / Accepted: date

Abstract A low voltage operating fully-differential CMOS OTA construction, which uses dual-input CMOS cascode inverters, is proposed. The OTA is a two-stage configuration with dual-input CMOS cascode inverters at the input stage, and traditional CMOS inverters in the output stage, with a common-mode feedback path from the output terminals to one of the input terminals of cascode inverters. In order to effectively reduce its threshold voltages by bulk bias technique, the OTA has been designed and fabricated by using a 0.15 μm triple-well CMOS process. The OTA successfully operated from 1-V power supply, with 59 dB of differential voltage gain, 80.9 dB of CMRR and 25 MHz of unity gain frequency, at 60 μA of current consumption.

Keywords 1-V operation · fully-differential OTA · CMOS cascode inverters

1 Introduction

There have been strong demands for low voltage and low power operating LSIs(large-scale integrated circuits) , in particular, portable or wearable equipments. Those naturally required to include digital signal processing blocks and analog functional circuit blocks like A-to-D, D-to-A converters, analog filters etc. on the same chip. The OPA(operational amplifiers) and OTA (operational transconductance amplifiers) are key building blocks to realize those analog functional blocks.

H. Tanimoto and K. Yazawa
Dept. of Electr. and Electronic Eng., Kitami Inst. of Technology, 165 Koen-cho, Kitami, Hokkaido, 090-8507 Japan
Tel.: +81-157-26-9278, Fax: +81-157-25-1087
E-mail: htanimot@mail.kitami-it.ac.jp

M. Haraguchi
Renesas Electronics Corp.,
4-1-3 Mizuhara, Itami, Hyogo, 664-0005 Japan

The digital blocks enjoy reduced power consumption by ever lowering supply voltage; however, many analog functional blocks do not function properly in low power supply voltages as low as 1 V. This paper presents a 1-V operating fully-differential OTA design and measured results of its test chip in 0.15 μm digital CMOS technology.

There are many reports on low voltage operation fully differential OTAs, operable as low as below 1 V [1–7]. For low voltage operation, we must care about input dead zone due to MOS threshold voltages and three-stacked structure of the differential pair circuit.

The low voltage operation itself is overcome by using complementary differential pairs[1,2], or using bulk driven differential pair[3,4], or introducing pseudo-differential amplifiers composed of NMOS or PMOS inverters [5–7]. However, their input common-mode range tends to be biased toward one side of the rails, and often do not include the mid-rail voltage, $V_{DD}/2$, which is desired at its output.

Consequently, those OTAs need additional common-mode level shift circuits in front of their input terminals and accommodate input common-mode voltage to output common-mode voltages. Typical strategies to overcome this issue may be summarized as follows:

- Using adaptive level shifters in front of complementary differential-stages to increase common-mode input range [1,2]. Those amplifiers have rail-to-rail input range; however, the level shifters require additional current sources and high resistances, which in turn increase power dissipation and thermal noise. This also prevents the amplifier to operate from the lower supply voltage.
- Using bulk driven differential pair to accommodate input common-mode signals[3,4]. This configuration has a wider input range; however, back gate has much lower transconductance than normal gate. Then, the amplifier tends to have low gain.

– Using active common-mode level shifters in front of pseudo differential amplifiers [6,7], or use common-mode feedback to stabilize output common-mode voltage [5]. This category has level shifting circuitry to shift the input common-mode range to include $V_{DD}/2$, however, still it has narrow common-mode input range. This limits their usage practically to inverting amplification.

In order to overcome this situation, the authors have proposed a two-stage fully-differential OTA configuration named "F/F-F/B(feedfoward-feedback) OTA", which consists only of CMOS inverters[8,9]. A CMOS inverter can be used as an analog voltage-controlled current-source, and unlike NMOS or PMOS inverters, it has rail-to-rail input range if $V_{DD} > V_{thn} + |V_{thp}|$ holds. Here, V_{DD} stands for power supply voltage, $V_{thn}(V_{thp})$ stands for NMOS(PMOS) threshold voltage. However, this OTA has about 50 dB of voltage gain at V_{DD} = 1.8 V[9], due to a low intrinsic gain of the deep submicron CMOS process[10,11].

In this paper, design details are described for a fully differential OTA with a lower operation voltage as low as 1 V and a higher voltage gain of 60 dB, by lowering V_{th} via bulk-bias effect[10], and using cascode inverter at the first stage. Measured results are also given for fabricated test chips.

2 Proposed OTA Configuration

In this section, we first discuss on the specific properties of F/F-F/B OTA structure. Then, a preferred OTA structure will be proposed.

2.1 F/F-F/B OTA Structure

The basic structure of F/F-F/B OTA[8] is shown in Fig. 1. An inverter symbol stands for a simple logic CMOS inverter, which is operating as a voltage controlled current-source (VCCS) in this OTA. The OTA is basically a two-stage balanced amplifier with common-mode rejection capability. The shaded portions in Fig. 1 are responsible for common-mode rejection function.

Since INV2 and INV3 (INV5 and INV6) act as an inverting amplifier of unity gain, the first stage of this OTA has a common-mode rejection capability by feedforward circuits, and differential-mode signals add up. The second stage also has common-mode rejection capability by a feedback circuit. Here, INV11, INV12, INV14, and INV15 consists an averaging circuit for +OUT and −OUT terminals to detect output common-mode signal. This is fed back via INV10 and INV13 to establish output common-mode stabilization. Note that this feedback loop is valid only for common-mode signals and does not affect to the output differential component.

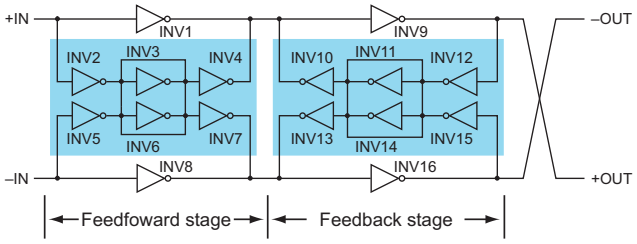

Fig. 1 Basic structure of F/F-F/B OTA [8]

The second stage may have Miller compensation capacitors to stabilize the total OTA.

2.2 Proposed OTA Configuration [12]

The above OTA successfully operated from 1.8 V power supply; however, its voltage gain is about 48 dB[8]. Because the OTA was designed by using inverters with minimum gate length, this led to a low voltage gain due to a low intrinsic gain of submicron CMOS devices used. The OTA also marginally operated from 1.0 V supply.

Our new goal is to design a fully differential OTA with higher voltage gain operating from 1.0 V power supply. To cope with these issues, we made use of the following facts for F/F-F/B OTA structure.

– Common-mode voltage of the second stage is practically kept constant at $V_{DD}/2$. This is a consequence of common-mode feedback, and the first stage sees low impedance for common-mode signal, while it sees high impedance for differential-mode signal.
– The first stage output need not swing large, because the second stage has a gain of 26 dB or so, and the output swing is less than 1 V_{p-p}. This corresponds to only about 50 mV_{p-p} swing at the first stage output.

From the above facts, we proposed to use cascode inverters for the first stage and enhance its voltage gain. Because the first stage inverters need to swing little, cascode inverters with four-stacked transistors can be used even for 1 V of power supply. The second stage uses normal inverters to assure a large output swing.

For the first stage inverters of F/F-F/B OTA structure, their output operating points are closely kept around $V_{DD}/2$, we may omit common-mode cancellation via feedforward circuit. Only the common-mode input range is of concern here.

For the second stage, large output voltage swing of 1 V_{p-p} requires a highly linear common-mode detecting amplifiers (INV12 and INV15 in Fig. 1). However, the output common-mode voltage must be kept around $V_{DD}/2$ for most situation. Therefore, we adopted a simple resistive common-mode detecting circuit. Fig. 2 shows the proposed OTA structure[12].

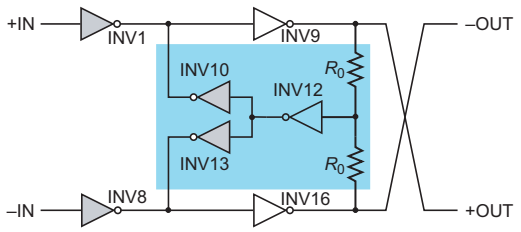

Fig. 2 Basic structure of proposed OTA [12]

This resistive common-mode detecting circuit slightly lowers the differential gain as low as 10%, because the output stage inverter has a low output impedance (see sections 3.2 and 3.3 for detail) .

The second stage of Fig. 2 has 100% common-mode feedback, and the first stage inverters see very low common-mode impedance, while they experience very high differential impedance at their output terminals. Also, cascode inverters are used for INV10 and INV13 to realize large differential gain in the first stage, because cascode inverters have much larger output impedance than ordinary inverters and have less loading effect.

For securing the OTA from instability, phase compensation must be considered separately in differential mode and common mode. This will be discussed in section 3.

2.3 Circuit Analysis of Proposed Configuration

Fig. 3 (a) shows a differential half-circuit of the proposed OTA shown in Fig. 2. The differential-mode voltage gain, A_{DM}, is calculated straight forward to be half of the cascaded inverters' voltage gain.

$$A_{\mathrm{DM}} = \frac{V_{\mathrm{outDM}}}{V_{\mathrm{inDM}}} = g_{\mathrm{m1}} \frac{r_{\mathrm{o1}}}{2} (g_{\mathrm{m2}} r_{\mathrm{o2}}) \tag{1}$$

Here, a factor 1/2 comes from output impedance of common-mode feedback circuit.

Fig. 3 (b) shows a common-mode half-circuit of the proposed OTA. Common-mode detecting resistor, R_0, is ignored for the sake of simplicity. Its input impedance looking into the second stage, Z_{in}, is calculated from the half circuit to be

$$Z_{\mathrm{in}} = \frac{r_{\mathrm{o1}}}{1 + g_{\mathrm{m1}} \frac{r_{\mathrm{o1}}}{2} (g_{\mathrm{m2}} r_{\mathrm{o2}})^2}. \tag{2}$$

That is, the output impedance of INV10 is divided by an open-loop gain of the common-mode feedback loop. The voltage gain of common-mode signal, A_{CM}, is calculated to be

$$A_{\mathrm{CM}} = \frac{V_{\mathrm{outCM}}}{V_{\mathrm{inCM}}} = g_{\mathrm{m1}} Z_{\mathrm{in}} (g_{\mathrm{m2}} r_{\mathrm{o2}}) \approx \frac{1}{g_{\mathrm{m2}} r_{\mathrm{o2}}}. \tag{3}$$

Then, common-mode rejection ratio, CMRR, can be calculated as follows.

$$\mathrm{CMRR} = \frac{A_{\mathrm{DM}}}{A_{\mathrm{CM}}} \approx \frac{1}{2} g_{\mathrm{m1}} r_{\mathrm{o1}} (g_{\mathrm{m2}} r_{\mathrm{o2}})^2 \tag{4}$$

This means that CMRR of the OTA is approximately equal to the loop gain of the three-stage common-mode feedback loop. This can be over 80 dB.

In conclusion, this OTA has a differential-mode gain of two-stage amplifier, and CMRR of the order of three-stage amplifier gain.

Another important observation is that voltage at node Ⓐ is kept almost $V_{\mathrm{DD}}/2$. Because the common-mode voltage is forced at $V_{\mathrm{DD}}/2$, and the differential-mode voltage may swing as small as $V_{\mathrm{DD}}/(g_{\mathrm{m2}} r_{\mathrm{o2}})$, say 50 mV or so. This means the first stage of the OTA has almost rail-to-rail input common-mode range, as a transconductor.

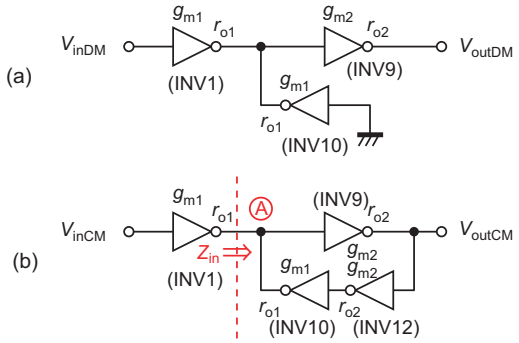

Fig. 3 Differential half-circuit (a), and common-mode half circuit (b)

3 Design Details

3.1 Low voltage cascode inverters

Cascode inverters are adopted with cascode transistors' back gates tied to their own sources, in order to obtain high voltage gain at low supply voltage. Also the common-source transistors' back gates are slightly forward biased to lower their effective threshold voltages as shown in Fig. 4(a). In Fig. 4(a), V_{G1} and V_{G2} are cascode transistor's bias voltages, and V_{B1} and V_{B2} are bulk bias voltages.

As shown in Fig. 2, INV1 and INV10 (INV8 and INV13) are cascode inverters and their outputs are tied together. Those inverters may be merged into a dual input version, in which the cascode transistors can be shared as shown in Fig. 4(b). This saves the chip area.

Test chips were fabricated by using Renesas Electronics' 0.15 μm CMOS process for microprocessors[13]. This is a 1.5 V triple-well process, and has free access to both NMOS and PMOS back gates. Threshold voltages of NMOS and

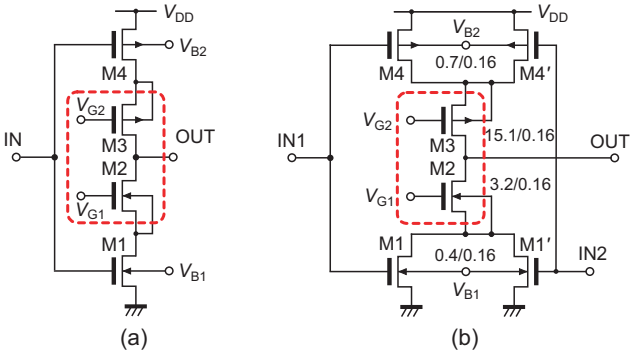

Fig. 4 Single input CMOS cascode inverter (a), and its dual input version with cascode transistors reused (b) [12]

PMOS transistors are around 0.35 V. From circuit simulation results, we decided to use $V_{B1} = 0.4$ V and $V_{B2} = 0.6$ V, that is, 0.4 V of forward bias for M1 and M4 in Fig. 4. This lowers both the threshold voltages about 70 mV. For cascode transistors, M2 and M3, their back gates are tied their own sources to cancel substrate bias effect.

The cascode transistors M2 and M3 are biased in saturation region at slightly off from the edge of triode region, in order to operate M1 and M4 mostly in saturation region by allocating V_{DS} as large as possible. Consequently, bias voltages for cascode transistors are set at $V_{G1} \approx 0.8$ V and $V_{G2} \approx 0.2$ V, with their $|V_{DS}| \approx 0.18$ V. This may allow M1 and M4 to have about $|V_{DS}| \approx 0.32$ V.

Because the cascode inverters are forced to operate at $V_{out} = 0.5$ V, M1 (M4) operates in saturation region within $V_{in} \leqq V_{DS} + V_{th} \approx 0.62$ V ($V_{in} \geqq 0.38$ V). Consequently, our cascode inverter will operate with both M1 and M4 in saturation region for $0.32 \text{ V} \leqq V_{in} \leqq 0.62$ V, and operate in triode region outside; however, triode operation will not cause serious problem, because the common-mode input impedance of the second stage is low. Designed aspect ratios (W/L) are given in Fig. 4(b), where, units are in μm.

3.2 Low voltage normal inverters

The output stage inverters are required to have high driving capability and large swing. The common-mode detector inverter must operate around $V_{DD}/2 = 0.5$ V, both its input and output terminals, when the OTA operates properly. Thus, normal inverters are adopted for output stage (INV9 and INV 16, in Fig. 2), and common-mode detection (INV12).

To lower the threshold voltages, the normal inverters are also forward biased by 0.4 V at their back gates.

The inverters INV9 and INV16 are designed to have large gate widths to drive nominal load of 50 kΩ || 5 pF, hence they have low output impedance. The inverters are carefully designed to have point symmetry about its quiescent point 0.5 V, by circuit simulation, to have aspect ratios of 8.1 μm/0.16 μm for PMOS and 3.6 μm/0.16 μm for PMOS. This resulted in 8.35 kΩ of output impedance for the output inverters.

The common-mode detection inverter is designed to have 2.47 μm/0.16 μm for PMOS and 0.5 μm/0.16 μm for NMOS.

3.3 Common-mode feedback

Design of common-mode feedback loop around the second stage is described in this section.

The common-mode detection resistors, R_0 in Fig. 2, may not be so large to avoid severe loading effect. A 100 kΩ resistor is used for R_0, considering its area on the chip. The resistive common-mode detecting circuit reduces differential voltage gain only about 0.4 dB, because the output resistance of INV9 and INV16 is about 8 kΩ.

The common-mode feedback loop include three inverters and must have phase compensation for its stability. This will be described in the next section.

3.4 Phase compensation

Final design of the OTA is shown in Fig. 5. The Miller compensation for INV9 and INV16 works both for differential-mode stability and common-mode stability, while C_2-R_2 compensation around INV12 affects only for common-mode stability. Also, C_0 is placed in parallel with common-mode detection resistor R_0 to introduce additional zero for better common-mode loop stability.

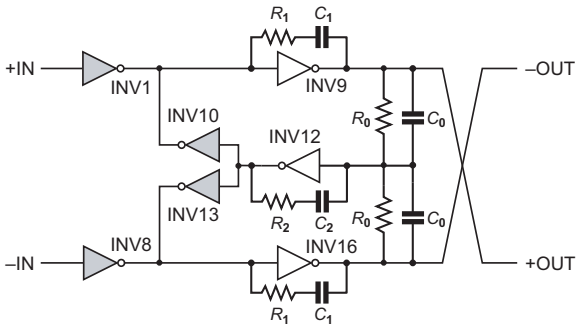

Fig. 5 Designed fully differential OTA with phase compensation [12]. $R_0 = 100$ kΩ, $C_0 = 50$ fF, $R_1 = 5$ kΩ, $C_1 = 0.5$ pF, $R_2 = 100$ kΩ, $C_2 = 0.1$ pF.

Table 1 shows the simulation results for the OTA's differential-mode characteristics. The results are simulated with 50 kΩ in parallel with 5 pF load at each output terminal, and $V_{CM} = 0.5$ V.

Fig. 6 shows layout design of the OTA. The die occupies an area of 226 μm $\times$ 138 μm. Three right hand rectangles are 100 kΩ resistors, and two rectangles at left side are 0.5 pF capacitors.

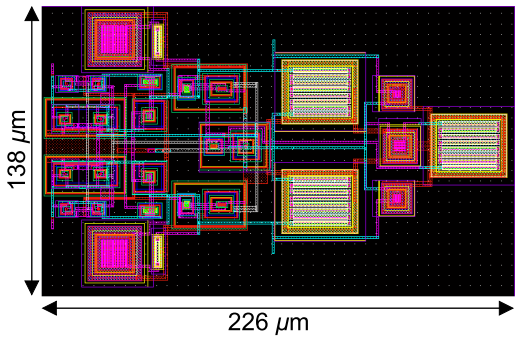

Fig. 6 Layout of designed OTA

Table 1 Simulated and measured results of designed OTA (V_{DD} =1.0 V)

	Simulated	Measured
Power supply voltage	1.0 V	1.0 V
Differential voltage gain	63.7 dB	59.0 dB
Common-mode voltage gain	−24.1 dB	−21.9 dB
CMRR	87.8 dB	80.9 dB
−3 dB freq.	20.5 kHz	32.0 kHz
Unity gain freq.	30.4 MHz	25.0 MHz
Current consumption	108.5 μA	59.9 μA
Output resistance	8.81 kΩ	–

4 Measured Results

A test chip was mounted on an evaluation PCB and measured. Unfortunately, an oscillation about 13 MHz was observed at the test chip outputs. After checking the evaluation PCB, we found that each OTA output terminal sees 12 pF of parasitic capacitance. Design of phase compensation assumed only 5 pF of capacitive load, so that compensation was not enough for this measurement setup.

By open-loop measurement with detaching output pins from the PCB to reduce capacitive loading, we were able to evaluate the OTA performance without oscillation.

4.1 Measurement setup [12]

Measurement setup for differential-mode gain is shown in Fig. 7. For common-mode gain measurement, Fig. 8 was used. The open-loop frequency responses are measured by using a spectrum analyzer and an active probe with 100 kΩ in prrarel with 3 pF of input impedance. The input common-mode dc operating point was set by externally through high resistances (DC+, in Figs. 7 and 8).

4.2 Measured results

4.2.1 1.0 V operation case [12]

Fig. 9 shows the measured frequency responses for V_{DD} = 1.0 V with input dc common-mode voltage V_{CM} = 0.5 V.

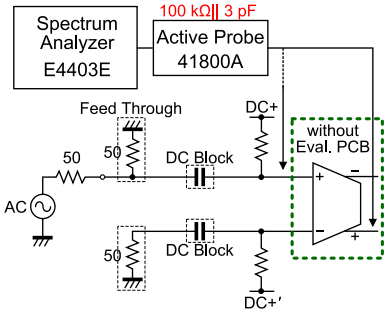

Fig. 7 Measurement setup for differential-mode gain

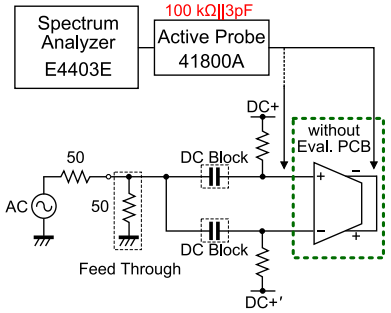

Fig. 8 Measurement setup for common-mode gain

The Fig. 9 also shows simulated responses with and without parasitic capacitors and resistors in the measurement setup. The results indicate close match of simulated and measured frequency responses both for differential-mode and common-mode. We see the common-mode gain has a peak at about 20 MHz, which is close to the oscillation frequency. Measured major characteristics are summarized in Table 1.

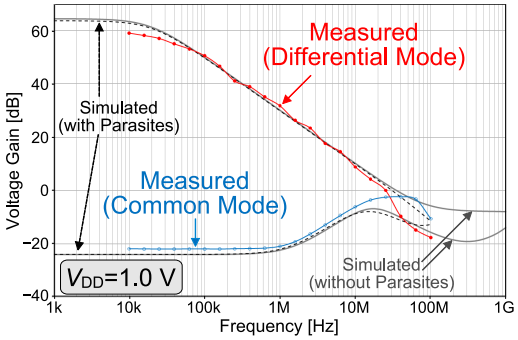

Fig. 9 Frequency responses of designed OTA (V_{DD} = 1.0 V) [12].

4.2.2 0.9 V and 1.1 V operation cases

In order to check robustness for power supply voltage change of the proposed OTA, we measured the chip at V_{DD} = 0.9 V and 1.1 V.

Fig. 10 and 11 show the measured frequency responses for V_{DD} = 0.9 V with input dc common-mode voltage V_{CM} =

0.45 V, and for V_{DD} = 1.1 V with input dc common-mode voltage V_{CM} = 0.55 V, respectively. Those figures also show simulated responses with parasitic capacitors and resistors in the measurement setup, in addition to reference simulated responses for V_{DD} = 1.0 V case.

Fig. 10 and 11 show similar curves for V_{DD} = 1.0 V operation; however, for V_{DD} = 0.9 V case, common-mode response shows clear peaking around 20 MHz, and differential-mode gain also has a small hump at that frequency. This may be a sign of marginal stability. So, the OTA needs more phase compensation for the common-mode loop.

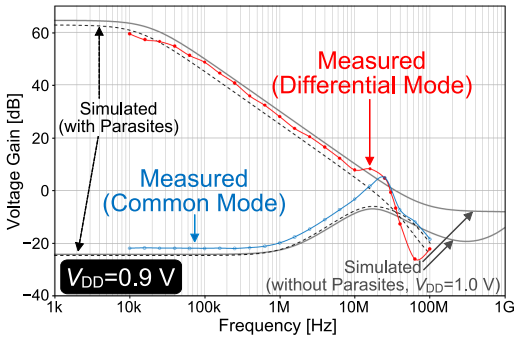

Fig. 10 Frequency responses of designed OTA (V_{DD} = 0.9 V).

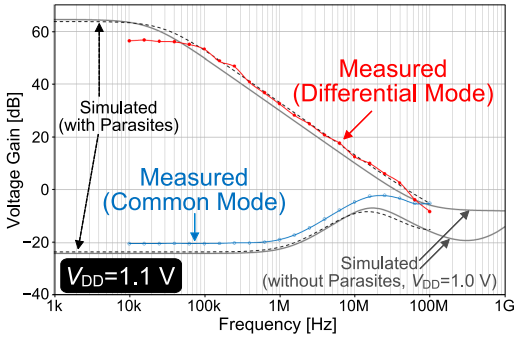

Fig. 11 Frequency responses of designed OTA (V_{DD} = 1.1 V).

For V_{DD} = 1.1 V operation, its current consumption is increased by about twice that of 1 V operation, and measured low frequency differential gain is lowered by about 3 dB, and −3 dB frequency is doubled.

Measured results for V_{DD} = 0.9 V, 1.0 V, 1.1 V are summarized in Table 2.

Table 2 Measured results of designed OTA (V_{DD} =0.9 V~ 1.1 V)

Supply voltage	1.1 V	1.0 V	0.9 V
Operating current	112 μA	59.9 μA	35.6 μA
Differential gain	56.4 dB	59.0 dB	59.3 dB
CMRR	76.4 dB	80.9 dB	81.1 dB
−3 dB frequency	66.7 kHz	32 kHz	26 kHz
Unity gain frequency	56.5 MHz	25 MHz	29.3 MHz

4.2.3 Common-mode input range [12]

Fig. 12 shows measured and simulated small-signal differential-mode and common-mode voltage gains versus input common-mode dc voltage. Against our expectation, common-mode input range is only about 0 V to 0.8 V, and does not extend to V_{DD} for positive rail side.

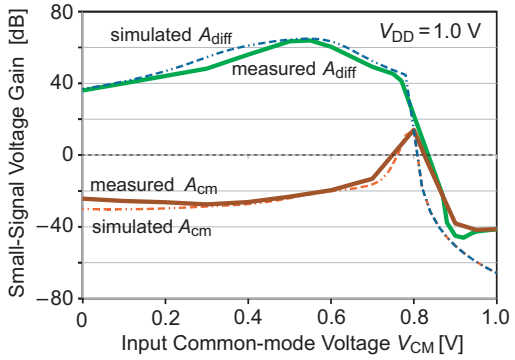

Fig. 12 Measured and simulated common-mode input range

4.2.4 T.H.D. and noise [12]

We have measured total harmonic distortion (T.H.D.) and noise performance of the test chip.

Fig. 13 shows the measured T.H.D. for open loop with no load. The OTA's single-end output voltage was measured by a spectrum analyzer via an active probe (Fig.7), then, T.H.D. was accumulated up to 10th harmonic components.

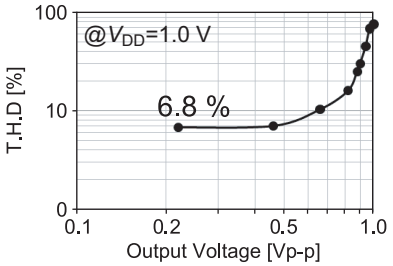

Fig. 13 Measured result of total harmonic distortion (up to 10th harmonics). f_{in} = 10 kHz, V_{CM} = 0.5 V.

Fig. 14 shows the measured input noise of the test chip. The equivalent input-noise is about 50 nV/ $\sqrt{\text{Hz}}$ for low frequency and raises to about 100 nV/ $\sqrt{\text{Hz}}$ around 1 MHz, then decreases to about 30 nV/ $\sqrt{\text{Hz}}$ at high frequency. The measured input noise resembles that of simulated result. The noise hump around 1 MHz appeared due to difference of decreasing slopes of OTA's voltage gain and output noise (Fig. 15). Note that the output noise measurement was a

single-ended measurement, and the output noise was refereed to input differential noise. This means that the equivalent input noise shown in Fig. 14 is a sum of differential input-noise and common-mode input-noise, while simulated input noise shows a pure differential-mode noise.

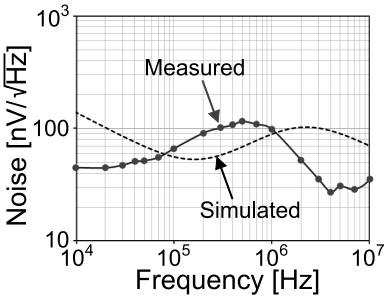

Fig. 14 Equivalent Input Noise of designed OTA (V_{DD} = 1.0 V)

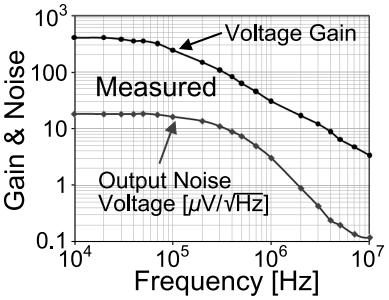

Fig. 15 Measured output noise and voltage gain (V_{DD} = 1.0 V)

5 Discussion

5.1 Oscillation in common-mode loop

At the very first evaluation, the test chip was mounted on a PCB, and we observed common-mode oscillation.

The reason for common-mode loop oscillation could be explained by the fact that the measured operating current of 59.9 μA was only 55% of the designed value for V_{DD} = 1 V (see Table 1), and thus, the inverters had narrower bandwidth. For V_{DD} = 0.9 V case, the situation becomes much worse and only 33% of operating current was supplied in comparison with the nominal operating current at 1 V operation (see Table 2).

For V_{DD} = 1 V operation, measured common-mode voltage gain is below 0 dB and the common-mode loop is stable. Under V_{DD} = 0.9 V condition, we observed small amplitude oscillation in common-mode, however, we could evaluate the test chips. A common-mode gain peak around 20 MHz in Fig. 10 may be an indication of oscillation.

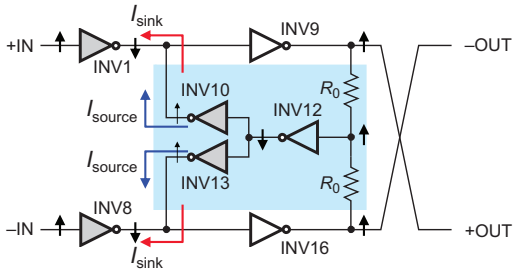

Fig. 16 Analysis of narrowed common-mode input range. I_{sink} > I_{source} is the situation.

The proposed OTA is based on CMOS inverters in class AB operation, which is much sensitive to V_{th} variation than class A amplifiers. This is a drawback of the use of CMOS inverter as an analog building block. We must be careful against processing variations by a design with sufficient phase margin.

5.2 Rail-to-rail common-mode input range

Form Fig. 12, the measured common-mode input range was 0 V to 0.8 V, and its higher side does not reach V_{DD}.

The point for this was analyzed as shown in Fig. 16. The reason is insufficient current absorbing capability of INV10 and INV13. Because there always exists some imbalance of output source/sink capability for INV1 (INV8), so that INV10 (INV13) could not absorb INV1's (INV8's) outgoing currents by its own in-taking currents enough to keep the OTA's output common-mode voltage around $V_{DD}/2$. Eventually, the common-mode feedback loop loses control of V_{out}.

It is important to recognize that this situation could easily be reversed, i.e, INV1 (INV8) may have larger sinking capability than sourcing capability, depending on the design. So, the inverters' source and sink capabilities should be designed to match each other.

Although we were not aware of the issue at the time of design, this could have easily been overcome, as circuit simulation shows, by just making INV10's (INV13's) gate width 1.5 to 2 times wider to enhance its current absorbing capability.

Figure 17 shows simulated V_{CM} versus small-signal voltage gain curves for the corrected design with twice the aspect ratio for INV10 and INV13, along with plots for the original design. As shown in the figure, we have rail-to-rail operation by the corrected design, although there is drop in differential gain of about 20 dB near at V_{CM} = 0 and V_{CM} = V_{DD}.

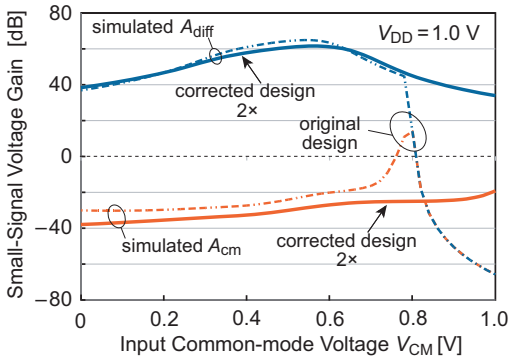

Fig. 17 Simulated common-mode input range for corrected design. "2×" indicates corrected designs.

5.3 Other issues

From Table 2, operating current dependence on supply voltage is fairly large. The operating current also varies with processing variation of threshold voltages of transistors. This is one of drawbacks of employing class AB CMOS inverters in the proposed OTA.

The operating current could be controlled if we employed conventional class A gain stages; however, this reproduces the issue of narrow common-mode input range again, which actually is overcome by using CMOS inverters.

One possible solution for the current variation issue may be controlling backgate biases of the output stage INV9 and INV16 to have desired operating current by a master-slave scheme[14], because those inverters consume most of the operating current. This solution may be applied to the cascode inverters as well.

Another issue is poor PSRR(power supply rejection ratio). As is well known, a standard CMOS inverter has a switching point voltage V_{SP} at which input and output voltages are equal. This voltage is designed to be $V_{SP} \approx V_{DD}/2$. For V_{SP}, the following relation holds[15]:

$$V_{SP} = \frac{V_{DD} - |V_{thp}| + V_{thn}\sqrt{\beta_n/\beta_p}}{1 + \sqrt{\beta_n/\beta_p}}, \tag{5}$$

where, V_{thx} is a threshold voltage and, β_x is a transconductance parameter, with subscript 'x' being n for NMOS and p for PMOS transistors. Eq. (5) indicates that V_{DD} and the threshold voltages are almost equally responsible to V_{SP}.

This indicates $\Delta V_{SP} \approx \Delta V_{DD}/2$ if threshohold voltages are independent of V_{DD} and $\sqrt{\beta_n/\beta_p} \approx 1$, then, ΔV_{SP} corresponds directly to the common-mode output voltage change, which leads to a poor PSRR. However, eq. (5) suggests that change in V_{SP} due to V_{DD} variation may be compensated by changing threshold voltages adaptively as in the case of [14]. Those issues are left for future work.

6 Conclusion

A 1-Volt operating fully-differential CMOS OTA based on cascode inverters in 0.15 μm CMOS process was designed and evaluated. For low voltage operation, CMOS inverters' bulks are slightly forward biased to effectively reduce their threshold voltages. Also, CMOS cascode inverters are used to enhance voltage gain of the OTA with minimum gate length. The fully-differential two-stage OTA construction was proposed with only the second-stage has a common-mode feedback loop inside. The OTA's first-stage was built with CMOS cascode inverters, while second-stage was built with conventional CMOS inverters. This enables both high gain and large output swing for rail-to-rail input.

The test chips are measured to have 59 dB of differential-mode voltage gain with 25 MHz unity gain frequency, and common-mode rejection ratio of 80.9 dB in 1-V operation. This demonstrates the usefulness of the proposed fully-differential OTA design.

Although the OTA aimed at rail-to-rail operation (0 V to 1 V) for common-mode input range, the test chip indicated 0 V to 0.8 V common-mode input range. This could easily be fixed by increasing cascode inverters' aspect ratio in the common-mode feedback loop.

In conclusion, we have shown the proposed circuit structure successfully operated from 1-V power supply with high differential gain within a wide common-mode input range. Issues associated with threshold voltage and supply voltage variations are future work.

Acknowledgments

The authors would like to thank Dr. Kazutami Arimoto and Yoshihiro Okuno, both of Renesas Electronics Corp., for their valuable discussion and providing an opportunity of making the test chip. The authors are also grateful to Yuki Fujioka, graduate student of Kitami Institute of technology, for his help in test chip measurement. The authors deeply thank Dr. Hideto Yanagisawa of Kitami Institute of Technology, for his assistance in preparing CAD design environment.

This work was partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design System, Inc.

References

1. Fonderie, J., Maris, M. M., Schnitger, E. J., Huijsing, J. H. (1989). 1-V Operational Amplifier with Rail-to-Rail Input and Output Ranges. *IEEE Journal of Solid-State Circuits*, 24(6), 1551–1559.
2. Duque-Carrillo, J. F., Ausín, J. L., Torelli, G., Valverde, J. M., Domínguez, M. A. (2000). 1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology. *IEEE Journal of Solid-State Circuits*, 35(1), 33–44.

3. Blalock, B. J., Allen, P. E., Rincon-Mora, G. A. (1998). Designing 1-V Op Amps Using Standard Digital CMOS Technology. *IEEE Trans. on Circuits and Systems–II*, 45(7), 769–780.
4. Stockstad, T., Yoshizawa, H. (2001). A 0.9-V 0.5-μA Rail-to-Rail CMOS Operational Amplifier. *IEEE Journal of Solid-State Circuits*, 37(3), 286–292.
5. Mohieldin, A. N., Sanchez-Sinencio, E., Silva-Martinez, J. (2003). A Fully Balanced Pseudo-Differential OTA With Common-Mode Feedforward and Inherent Common-Mode Feedback Detector. *IEEE Journal of Solid-State Circuits*, 38(4), 663–668.
6. Ueno, T., Itakura, T. (2004). A 0.9V 1.5mW continuous-time $\Delta\Sigma$ modulator for WCDMA. *IEEE International Solid-State Circuits Conference*, XLVII, 78–79.
7. Chatterjee, S., Tsividis, Y., Kinget, P. (2005). A 0.5 V Filter with PLL-Based Tuning in 0.18 μm CMOS. *IEEE International Solid-State Circuits Conference*, XLVIII, 506–507.
8. Komoriyama, K., Yoshida, E., Yashiki, M., Tanimoto, H. (2007). A Very Wideband Fully Balanced Active RC Polyphase Filter Based on CMOS Inverters in 0.18 um CMOS Technology. *Symposium on VLSI Circuits*, 10-2.
9. Komoriyama, K., Yashiki, M., Yoshida, E., Tanimoto, H. (2008). A VeryWideband Active RC Polyphase Filter with Minimum Element Value Spread Using Fully Balanced OTA Based on CMOS Inverters. *IEICE Trans. Electronics*, E91-C(6), 879–886.
10. Razavi, B. (2001). *Design of Analog CMOS Integrated Circuits*, Chapt. 3, McGraw-Hill, New York.
11. Annema, A., Nauta, B., van Langevelde, R., Tuinhout, H. (2005). Analog Circuits in Ultra-Deep-Submicron CMOS. *IEEE Journal of Solid-State Circuits*, 40(1), 132–143.
12. Tanimoto, H., Yazawa, K., Haraguchi, M. (2012). A 1-V Operating CMOS Fully-Differential OTA Based on Cascode Inverters. *2012 International Conference on Analog VLSI Circuits*, Valencia, Spain, ISBN: 978-84-695-5457-9.
13. Shinji Kawai et al., "An 8kB EEPROM-Emulation Data FLASH Module for Automotive MCU," *IEEE ISSCC 2008 Digest of Technical Papers*, 28.2, SanFrancisco, U.S.A., Feb. 2008.
See also: http://dx.doi.org/10.1109/ISSCC.2008.4523280/mm1
14. Vlassis, S. (2012) "0.5 V CMOS inverter-based tunable transconductor," *Analog Integrated Circuits and Signal Processing*, VOl. 72, pp. 289–292. DOI 10.1007/s10470-012-9865-0
15. Baker, R. J. (2010), *CMOS Circuit Design, Layout, and Simulation (book)*, Third Ed., Chapt. 11, John Wiley& Sons, Inc., Hoboken, New Jersey, ISBN:978-0-470-88132-3.