VLSI Design of an Interference Canceller for QPSK OFDM-IDMA Systems

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***Abstract*—With growing demand of machine to machine (M2M) communication, wireless communication systems request simultaneous connections for many terminals to cope with thus increasing communication throughput. We focus on interleave division multiple access (IDMA) that has superior user detection performance and describe a VLSI design of an interference canceller that performs user detection in QPSK OFDM-IDMA systems. A conventional interference canceller has an issue of degradation in interleave memory throughput. We propose a new architecture of dual-frame processing in an interference canceller by making use of an OFDM-IDMA frame structure. In FPGA implementation, the proposed architecture has shown fewer hardware resources compared with the conventional architecture.**

I. Introduction

In recent years, M2M (Machine to Machine) network that autonomously exchanges information among machines via a network has attracted attention and become an essential technology to construct information infrastructures such as smart cities and smart grids [1], [2]. Wireless communication systems request simultaneous connections for many terminals to cope with thus increasing communication throughput. Multiple access, simultaneously connecting multiple user terminals, is classified into orthogonal and non-orthogonal schemes in radio resource allocation. Orthogonal multiple access that each user separates radio resources by time and frequency units as FDMA, TDMA, and OFDMA, requires scheduling where control information is exchanged among base stations and user terminals. On the other hand, non-orthogonal multiple access as CDMA and interleave division multiple access (IDMA) [3] does not require the scheduling. IDMA is superior to CDMA in multiuser detection (detecting desired signals from interference and noise) on the condition of connecting many users [4]. Furthermore, OFDM-IDMA [5] executing a channel equalization in frequency domain is effective under multipath fading environment, where throughput evaluation in cellular communication [6] and hardware development and outdoor experiment [7], [8] have been studied.

This paper describes a VLSI design of an interference canceller that is the most important part in OFDM-IDMA processing. The interference canceller separates user signals by iterative processing, whose computational cost is proportional to the numbers of users and iterations. As a conventional architecture, pipeline and parallel interference canceller has been presented in a partitioned spreading CDMA (PS-CDMA) receiver [9]. The conventional architecture decreases a throughput processing due to wait time occurring in interleave and deinterleave memory units, whose utilization ratio in circuit operation is half. The proposed architecture adopts dual-frame processing to solve the problem of the wait time and achieves a high utilization ratio, which can reduce more hardware resources in VLSI implementation. Since the interference canceller for BPSK transmission mode has been designed in our previous work [7], we present a new design for QPSK transmission mode.

II. OFDM-IDMA System

A. Transmitter and Receiver

Block diagrams of OFDM-IDMA transmitter and receiver and uplink channel are shown in Fig. 1. In the transmitter in Fig. 1(a), the coded bit sequence $\boldsymbol{c}_k$=[$c_k(0)$,$c_k(1)$,...,$c_k(n)$,...,$c_k(N-1)$] $\in \{0,1\}(0 \leq n \leq N-1)$ is generated by N_{rep}-times repetition codes with a coding rate R_{rep}(=$1/N_{\mathrm{rep}}$) from the information bit sequence $\boldsymbol{b}_k$=[$b_k(0)$,$b_k(1)$,...,$b_k(n_{\mathrm{b}})$,...,$b_k(N_{\mathrm{b}}-1)$] $\in \{0,1\}(0 \leq n_{\mathrm{b}} \leq N_{\mathrm{b}}-1)$. n_{b} is a bit number in the information bit sequence and N(=$N_{\mathrm{b}}N_{\mathrm{rep}}$) denotes the number of symbols, and k ($0 \leq k \leq K-1$) indicates a user number. The transmit symbol sequence $\tilde{\boldsymbol{c}}_k$ is generated by changing the order of the coded bits by adopting a user specific interleaving pattern π_k. The QPSK symbol sequence $\boldsymbol{x}_k$=[$x_k(0)$,$x_k(1)$,...,$x_k(n)$,...,$x_k(N-1)$] is generated by a QPSK modulator. Those symbols are allocated in frequency and time slots within an OFDM packet. After the OFDM modulation, the OFDM-IDMA signals $\bar{\boldsymbol{x}}_k$ are transmitted by adding a cyclic prefix (CP).

In the uplink channel in Fig. 1(b), the OFDM-IDMA transmitted signals $\bar{\boldsymbol{x}}_k$ are multiplied by the channel coefficient $\bar{\boldsymbol{h}}_k$ for each user. The OFDM-IDMA received signals $\bar{\boldsymbol{y}}$ are modeled by summing the channel affected signals of all users. In the receiver in Fig. 1(c), the frequency-domain received signals $\boldsymbol{y}$ are obtained by the removal of CPs and the OFDM demodulation. From the training signals located at the head of OFDM packet, the channel coefficients of all users $\boldsymbol{h}_0$,$\boldsymbol{h}_1$,...,$\boldsymbol{h}_{K-1}$ are computed by the frequency-domain channel estimation. The interference canceller consists of the elementary signal estimator (ESE) and the parallel iterative decoders (DECs) with K users [10]. The number of iterations is given by N_{iter}. The ESE computes the extrinsic value $\lambda_{\mathrm{dec}}(\tilde{\boldsymbol{c}}_k)$ for each user by using the received signals $\boldsymbol{y}$ and the channel coefficients of all users $\boldsymbol{h}_0$,$\boldsymbol{h}_1$,...,$\boldsymbol{h}_{K-1}$. The DEC accepts the extrinsic value $\lambda_{\mathrm{mud}}(\boldsymbol{c}_k)$ after deinterleaving π_k^{-1} and outputs the information bit sequence $\boldsymbol{b}_k$ by decoding of repetition codes with QPSK demodulation. The reliable extrinsic value $\lambda_{\mathrm{dec}}(\boldsymbol{c}_k)$ converts to $\lambda_{\mathrm{dec}}(\tilde{\boldsymbol{c}}_k)$ by interleaving π_k. The converted data $\lambda_{\mathrm{dec}}(\tilde{\boldsymbol{c}}_k)$ is used as the input of ESE at the next iteration step.

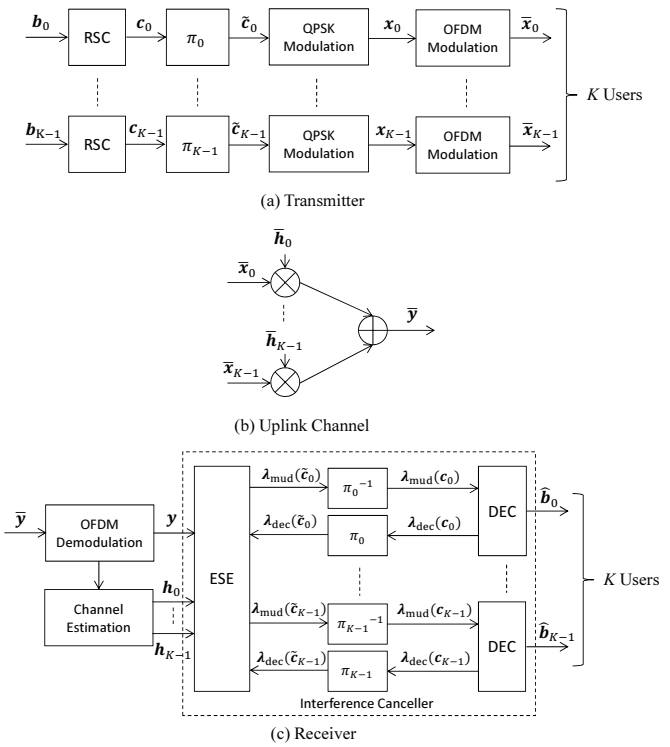

Fig. 1. Block diagrams of OFDM-IDMA transmitter and receiver and uplink channel.

B. Interference Canceller

The interference cancellation by an iterative processing is given by the following procedure:
(A) Generate the inputs of the interference canceller by interleaving the extrinsic values of the decoder outputs.

$$\lambda_{\rm dec}(\tilde{\boldsymbol{c}}_k) = \pi_k(\lambda_{\rm dec}(\boldsymbol{c}_k)), \tag{1}$$

where $\lambda_{\rm dec}(\boldsymbol{c}_k) = \boldsymbol{0}$ is applied in case of the first iteration step.
(B) Compute the expectation and variance values of the desired signals as $E_k(n)$ and $V_k(n)$ and their summations as $\bar{E}(n)$ and $\bar{V}(n)$. The symbol index n is divided into odd and even numbers of $2m$ and $2m-1$ ($0 \le m \le N/2-1$), their equations are given by

$$E_k(m) = h_k(m)\{\tanh(\lambda_{\rm dec}(\tilde{c}_k(2m))/2) + j\tanh(\lambda_{\rm dec}(\tilde{c}_k(2m+1))/2)\} \tag{2}$$

$$V_k(m) = (1 - {\rm Re}[E_k(m)]^2) + j(1 - {\rm Im}[[E_k(m)]^2) \tag{3}$$

$$\bar{E}(m) = \sum_{k=0}^{K-1} E_k(m) \tag{4}$$

$$\bar{V}(m) = \sum_{k=0}^{K-1} V_k(m), \tag{5}$$

where ${\rm Re}[\cdot]$ and ${\rm Im}[\cdot]$ indicate extracting real and imaginary parts, respectively.
(C) Compute the outputs of the ESE as $\lambda_{\rm mud}(\tilde{\boldsymbol{c}}_k)$ by log likelihood ratios (LLRs).

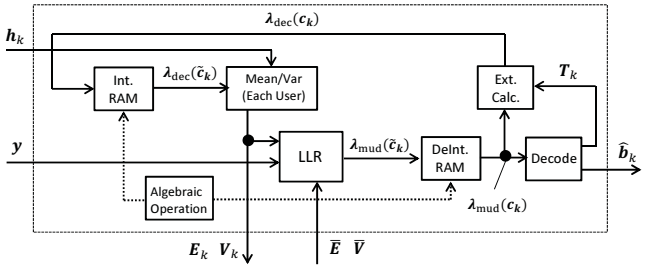

Fig. 2. Conventional architecture.

$$E'_k(m) = x_k(m) - \bar{E}(m) + E_k(m) \tag{6}$$

$$V'_k(m) = \bar{V}(m) - V_k(m) + (1+j)\sigma \tag{7}$$

$$\lambda_{\rm mud}(\tilde{c}_k(2m)) = \frac{2|h_k(m)|^2 \cdot {\rm Re}[E'_k(m)h^*_k(m)]}{{\rm Re}[h^*_k(m)]^2{\rm Re}[V'_k(m)] + {\rm Im}[h^*_k(m)]^2{\rm Im}[V'_k(m)]} \tag{8}$$

$$\lambda_{\rm mud}(\tilde{c}_k(2m+1)) = \frac{2|h_k(m)|^2 \cdot {\rm Im}[E'_k(m)h^*_k(m)]}{{\rm Re}[(h^*_k(m)]^2{\rm Im}[V'_k(m)] + {\rm Im}[(h^*_k(m)]^2{\rm Re}[V'_k(m)]}, \tag{9}$$

where σ denotes the average noise power in the received signals and the outputs of $\lambda_{\rm mud}(\tilde{c}_k(2m))$ and $\lambda_{\rm mud}(\tilde{c}_k(2m+1))$ are merged by the original order of symbol index m.
(D) Generate the DEC inputs as $\lambda_{\rm mud}(\boldsymbol{c}_k)$ by deinterleaving.

$$\lambda_{\rm mud}(\boldsymbol{c}_k) = \pi_k^{-1}(\lambda_{\rm mud}(\tilde{\boldsymbol{c}}_k)) \tag{10}$$

(E) Compute the DEC outputs as $\hat{\boldsymbol{b}}_k$ and the extrinsic values for the next iteration as $\lambda_{\rm dec}(\boldsymbol{c}_k)$.

$$T_k(n_{\rm b}) = \sum_{n_{\rm rep}=0}^{N_{\rm rep}-1} \lambda_{\rm mud}(c_k(n_{\rm rep} + N_{\rm rep}n_{\rm b})) \tag{11}$$

$$\hat{b}_k(n_{\rm b}) = f_{\rm Demod}(T_k(n_{\rm b})) \tag{12}$$

$$\lambda_{\rm dec}(\boldsymbol{c}_k) = \{T_k(0), ..., T_k(n_{\rm b}), ..., T_k(N_{\rm b}-1)\} - \lambda_{\rm mud}(\boldsymbol{c}_k), \tag{13}$$

where $n = n_{\rm rep} + N_{\rm rep}n_{\rm b}$ ($0 \le n_{\rm b} \le N_{\rm b}-1$). $f_{\rm Demod}$ generates binary data by QPSK demodulation. By repeating the aforementioned procedure, the decoder output sequence $\hat{\boldsymbol{b}}_k$ gradually approaches to the information bit sequence $\boldsymbol{b}_k$.

III. VLSI Design of Interference Canceller

A. Architecture

Conventional architecture based on pipeline processing that has been used in PS-CDMA system [9] is illustrated in Fig. 2. All circuit blocks operate by pipeline processing and the feedback datapath of $\lambda_{\rm dec}(\boldsymbol{c}_k)$ realizes iterative processing. We have modified the mean and variance computation block ("Mean/Var") and the LLR computation block ("LLR") for IDMA. Also, we use the algebraic interleaver, where the address generation is executed in the "Algebraic Operation" block [7]. When the outputs of the extrinsic value computation block "Ext. Calc" go back to the input of the interleaver memory ("Int. RAM"), the next iterative process is started.

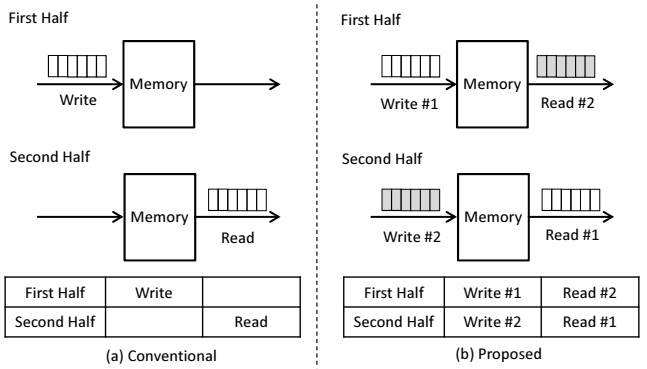

Fig. 3. Timings of memory read and write operations.

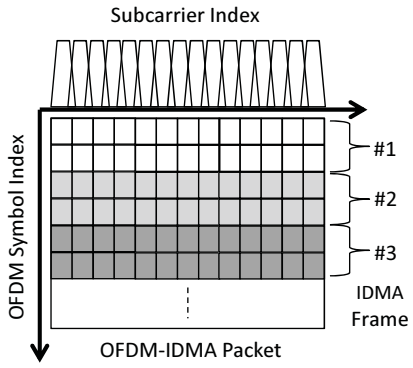

Fig. 4. OFDM-IDMA packet format.

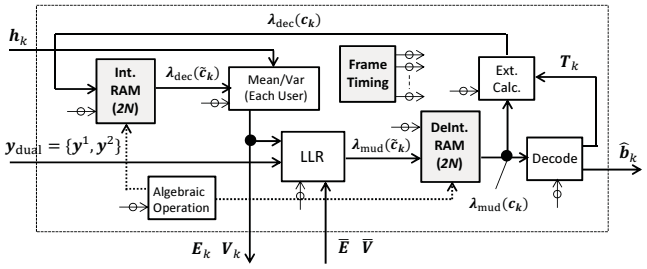

Fig. 5. Proposed architecture.

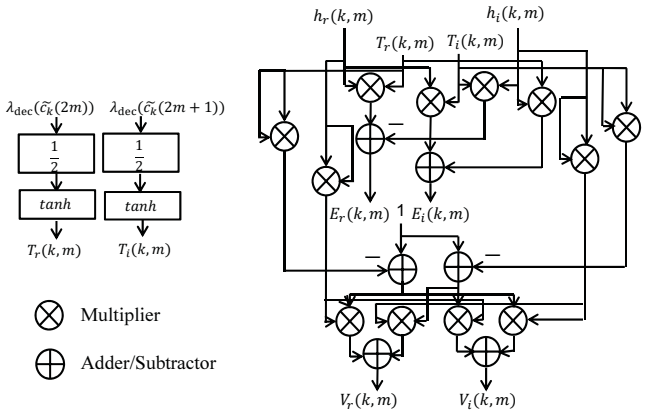

Fig. 6. Circuit structure of expectation and variance computation.

Timings of memory read and write operations in conventional and proposed architectures are shown in Fig. 3. In the conventional architecture of Fig. 3(a), the memory reading cannot start until the memory writing for the whole data has finished. Originally, operations of interleaver and deinterleaver are not compatible with pipeline processing. To avoid this incompatibility, we introduce dual-frame processing in the proposed architecture. Considering an OFDM-IDMA packet format shown in Fig. 4, multiple IDMA frames have been allocated in OFDM symbol and subcarrier indexes. Since these IDMA frames have the identical symbol index and data order, the interference canceller can process two frames by filling up the blank intervals, as shown in Fig. 3(b). The simultaneous operations of memory reading and writing are easily realized by use of dual-port memory. The proposed architecture is illustrated in Fig. 5. It expands the interleaver and deinterleaver memory sizes to $2N$ words. The additional circuit block supplying the dual-frame timings are requested, however, most of arithmetic units are the same with those in the single-frame processing.

Table I compares conventional and proposed architectures in the number of operation cycles, throughput, and memory size per user. F denotes clock frequency (Hz) and τ is the number of latency cycles caused by pipeline stages. $W_{\rm D}$ denotes a bit length in fixed-point operation. The proposed architecture provides a throughput of twice higher than the conventional architecture. The proposed architecture costs a double memory size, however fewer hardware resources than the conventional architecture on the same throughput condition.

B. Complex Arithmetic Unit

The computations of mean and variance values in (2)-(5) and LLRs in (6)-(9) require complex operations in arithmetic units. We define real and imaginary parts of $\boldsymbol{y}$ and $\boldsymbol{h}_k$ as

$$y_{\rm r}(m) = {\rm Re}[y(m)] \quad (14)$$
$$y_{\rm i}(m) = {\rm Im}[y(m)] \quad (15)$$
$$h_{\rm r}(k,m) = {\rm Re}[h_k(m)] \quad (16)$$
$$h_{\rm i}(k,m) = {\rm Im}[h_k(m)]. \quad (17)$$

We convert the complex operations to only real operations that can be implemented by fixed-point arithmetic units, expressed by the following equations:

$$T_{\rm r}(k,m) = h_{\rm r}(k,m)\tanh(\lambda_{\rm dec}(\tilde{c}_k(2m))/2)) \quad (18)$$
$$T_{\rm i}(k,m) = h_{\rm i}(k,m)\tanh(\lambda_{\rm dec}(\tilde{c}_k(2m+1))/2)) \quad (19)$$
$$E_{\rm r}(k,m) = h_{\rm r}(k,m)T_{\rm r}(k,m) - h_{\rm i}(k,m)T_{\rm i}(k,m) \quad (20)$$
$$E_{\rm i}(k,m) = h_{\rm r}(k,m)T_{\rm i}(k,m) + h_{\rm i}(k,m)T_{\rm r}(k,m) \quad (21)$$

$$V_{\rm r}(k,m) = h_{\rm r}^2(k,m)(1-T_{\rm r}^2(k,m)) + h_{\rm i}^2(k,m)(1-T_{\rm i}^2(k,m)) \quad (22)$$
$$V_{\rm i}(k,m) = h_{\rm i}^2(k,m)(1-T_{\rm r}^2(k,m)) + h_{\rm r}^2(k,m)(1-T_{\rm i}^2(k,m)) \quad (23)$$
$$\bar{E}_{\rm r}(m) = \sum_{k=0}^{K-1} E_{\rm r}(k,m) \quad (24)$$
$$\bar{E}_{\rm i}(m) = \sum_{k=0}^{K-1} E_{\rm i}(k,m) \quad (25)$$

TABLE I. COMPARISON OF ARCHITECTURE

	Conventional	Proposed
Operation cycle	$N_{\rm iter}(2N+\tau)+N$	$N_{\rm iter}(2N+\tau)+N$
Throughput (bits/s)	$2FN_{\rm b}/(N_{\rm iter}(2N+\tau)+N)$	$4FN_{\rm b}/(N_{\rm iter}(2N+\tau)+N)$
Memory bit (bits)	$4W_{\rm D}N$	$8W_{\rm D}KN$

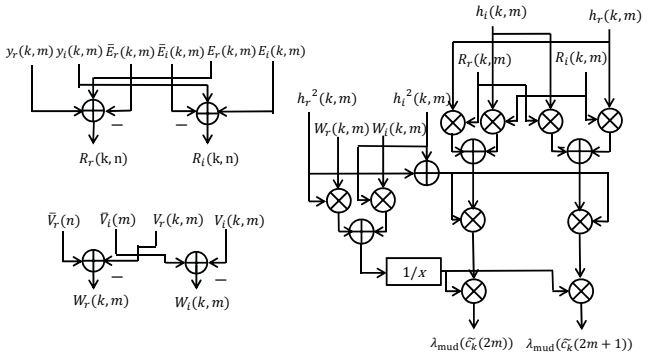

Fig. 7. Circuit structure of LLR computation.

TABLE II. IMPLEMENTATION RESULTS.

	Conventional	Conventional (2 units)	Proposed
Clock Frequency (MHz)	116.7	116.7	104.4
Registers	609	1,218	638
LUTs	1,264	2,528	1,453
Slices	418	836	511
RAMs (36kb)	8	16	16
DSP Slices	38	76	38
Operation cycles	86,336	86,336	86,336
Throughput (bits/s)	1.38 M	2.76 M	2.48 M
Memory bit (bits)	0.26 M	0.52 M	0.52 M

$$\bar{V}_{\rm r}(m)=\sum_{k=0}^{K-1}V_{\rm r}(k,m)+\sigma \tag{26}$$

$$\bar{V}_{\rm i}(m)=\sum_{k=0}^{K-1}V_{\rm i}(k,m)+\sigma \tag{27}$$

$$R_{\rm r}(k,m)=y_{\rm r}(k,m)-\bar{E}_{\rm r}(m)+E_{\rm r}(k,m) \tag{28}$$

$$R_{\rm i}(k,m)=y_{\rm i}(k,m)-\bar{E}_{\rm i}(m)+E_{\rm i}(k,m) \tag{29}$$

$$W_{\rm r}(k,m)=\bar{V}_{\rm r}(m)-V_{\rm r}(k,m) \tag{30}$$

$$W_{\rm i}(k,m)=\bar{V}_{\rm i}(m)-V_{\rm i}(k,m) \tag{31}$$

$$\lambda_{\rm mud}(\tilde{c}_k(2m))=4R_{\rm r}(k,m)\times \frac{(h_{\rm r}(k,m)+R_{\rm i}(k,m)h_{\rm i}(k,m))(h_{\rm r}^2(k,m)+h_{\rm i}^2(k,m))}{W_{\rm r}(k,m)h_{\rm r}^2(k,m)+W_{\rm i}(k,m)h_{\rm i}^2(k,m)} \tag{32}$$

$$\lambda_{\rm mud}(\tilde{c}_k(2m+1))=-4R_{\rm r}(k,m)\times \frac{(h_{\rm i}(k,m)+R_{\rm i}(k,m)h_{\rm r}(k,m))(h_{\rm r}^2(k,m)+h_{\rm i}^2(k,m))}{W_{\rm r}(k,m)h_{\rm r}^2(k,m)+W_{\rm i}(k,m)h_{\rm i}^2(k,m)}. \tag{33}$$

Circuit structures of expectation and variance computation in (18)-(27) and LLR computation in (28)-(33) are illustrated in Figs 6 and 7. Since all fixed-point arithmetic units are working by pipeline processing, their units do not decrease a throughput of the interference canceller.

IV. IMPLEMENTATION

The implementation results of proposed and conventional architectures based on Xilinx FPGA XC7K325T are summarized in Table II. We set a pipeline latency to τ=39 and a bit length in fixed-point format to W_D=16. Since the throughput value of the conventional architecture is about half as that of the proposed architecture, we evaluate the circuit by the condition that two interference cancellers are used in the conventional architecture. In this condition, the proposed architecture has reduced hardware resources in registers, LUTs, slices, and DSP slices by about 40 to 50%, compared with the conventional architecture.

V. SUMMARY

This paper has presented the VLSI design of interference canceller for QPSK OFDM-IDMA systems. We have applied dual-frame processing to solve an issue of decreasing an utilization ratio in interleave and deinterleave memory blocks. In the FPGA implementation, the proposed architecture has shown fewer hardware resources than the conventional architecture.

REFERENCES

[1] Steve Whitehead, "Adopting wireless machine-to-machine technology," IEE Computing and Control Engineering, Vol.15, No.5, pp.40-46, Oct. 2004.

[2] Inhyok Cha, Yogendra Shah, Andreas U. Schmidt, Andreas Leicher, Michael Victor (Mike) Meyerstein, "Trust in M2M communication," IEEE Vehicular Technology Magazine, Vol. 4, No. 3, pp. 69-75, Sept. 2009.

[3] Li Ping, Lihai Liu, Keying Wu, W. K. Leung, "Interleave-division multiple access," IEEE Transaction on Wireless Communication, Vol. 5, No. 4, pp. 938-947, Apr. 2006.

[4] Katsutoshi Kusume, Gerhard Bauch, Wolfgang Utschick, IDMA vs. CDMA: analysis and comparison of two multiple access schemes," IEEE Transactions on Wireless Communications, Vol.11, Issue 1, pp.78-87, Jan. 2012.

[5] Li Ping, Qinghua Guo, Jun Tong, "The OFDM-IDMA approach to wireless communication systems," IEEE Wireless Communications, Vol. 14, Issue. 3, pp. 18-24, June 2007.

[6] Tomoko Matsumoto, Yasuyuki Hatakawa, Satoshi Konishi, "Performance analysis of interleave-division multiple access for uplink in multi-cell environment," IEEE International Wireless Communications and Mobile Computing Conference (IWCMC), pp. 376–381, July 2011.

[7] Shingo Yoshizawa, Yasuyuki Hatakawa, Tomoko Matsomoto, Satoshi Konishi, Yoshikazu Miyanaga, "Hardware implementation of an interference canceller for IDMA wireless communications," IEEE International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), pp.645–650, Nov. 2013.

[8] Yuki Hikiyama, Hiroki Iwaizumi, Shingo Yoshizawa, Yasuyuki Hatakawa, Satoshi Konishi, Hiroshi Tsutsui, Yoshikazu Miyanaga, "Channel evaluation of IDMA in outdoor transmission experiment," Proceedings of the 2014 IEICE General Conference, B-5-45, pp. 440, Mar. 2014.

[9] Russell Dodd, Christian Schlegel, Vincent Gaudet, "DS-CDMA implementation with iterative multiple access interference cancellation," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 60, Issue 6, pp. 222-231, Jan 2013.

[10] Li Ping, Lihai Liu, W. K. Leung, "A simple approach to near-optimal multiuser detection: Interleave-division multiple-access," IEEE Wireless Communications and Networking Conference (WCNC), Vol. 1, pp. 391–396, March 2003.